Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY
Winter Examination-2018

Subject Name: VLSI Technology

Subject Code: 4TE07VLT1 Branch: B.Tech (EC)

Semester: 7 Date: 29/11/2018 Time: 10:30 To 01:30 Marks :70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt all questions** **(14)**

a) Draw the more simplified view of VLSI design flow.
b) Define the terms regularity and modularity.
c) State the different criteria used for measure the design quality for chip design.
d) Define the term Dual In Line Package.
e) Define the terms Positive photoresist and negative photoresist.
f) Define the term photo lithography.
g) State the type of Fermi level potential for n-type and p-type silicon substrate.
h) Define the term work function.
i) Define the term threshold voltage $V_{TO.}$
j) Define the terms Enhancement and Depletion mode MOSFET.
k) NM_L
l) NM_H
m) Define the term controllability
n) Define the term obsrevability

Attempt any four questions from Q-2 to Q-8

Q-2 **Attempt all questions** **(14)**

(a) Explain in detail with diagrams VLSI Design flow. **07**
(b) Write short notes on 'packaging technology used in VLSI chips'. **07**

Q-3 **Attempt all questions** **(14)**

(a) Why do we require device isolation between MOS transistors that comprise an IC? Explain LOCOS isolation technique with necessary diagrams. **07**
(b) Explain the band diagram of MOS Structure at surface inversion and derive the expression for threshold voltage. **07**

Q-4 **Attempt all questions** **(14)**

(a) With neat sketch explain gradual channel approximation and derive the equation for drain current in linear region mode and saturation mode for MOSFET. **07**
(b) Explain in detail effect of channel length modulation and substrate bias on drain current of NMOS transistor. **07**

Q-5		**Attempt all questions**	**(14)**
	(a)	Draw circuit of Resistive load inverter. Derive V_{IL}, V_{IH} and V_{OL} for resistive load inverter.	**07**
	(b)	Draw the combinational logic circuit using nMOS for the following Boolean expression: (i) Z1 = (A(B+C) + DE)' (ii) Z2= ((A+D+E)+(BC))'	**07**
Q-6		**Attempt all questions**	**(14)**
	(a)	Draw and discuss three stage ring oscillator circuit.	**07**
	(b)	Draw CMOS implementation of the D-latch with two-inverter loop and two CMOS TG switches. Explain in detail its working.	**07**
Q-7		**Attempt all questions**	**(14)**
	(a)	Explain the voltage bootstrapping in Dynamic logic circuits.	**07**
	(b)	Explain the basic principles of pass transistor circuits. Also explain logic "0" and logic "1" transfer.	**07**
Q-8		**Attempt all questions**	**(14)**
	(a)	Discuss in detail with diagrams the on-chip clock generation and distribution.	**07**
	(b)	Write short note on Ad hoc testable design techniques.	**07**